CMT211xA Schematic and PCB Layout Design Guideline

1. Introduction

The purpose of this document is to provide the guidelines to design a low-power CMT211xA transmitter with the maximized output power, minimized spurious emissions and optimized harmonics rejection. The products covered in this document are listed in the table below.

Table 1. Products Covered in this Document

Product	Frequency	Modulation	Tx Current Consumption	Configuration	1-wire Interface
CMT2110A	240-480 MHz	OOK	13.4 mA (+10 dBm, 433.92 MHz, OOK)	EEPROM	✓
CMT2113A	240-480 MHz	(G)FSK/OOK	23.5 mA (+10 dBm, 433.92 MHz, FSK)	EEPROM	✓
CMT2117A	240-960 MHz	OOK	15.5 mA (+10 dBm, 868.35 MHz, OOK)	EEPROM	✓
CMT2119A	240-960 MHz	(G)FSK/OOK	27.6 mA (+10 dBm, 868.35 MHz, FSK)	EEPROM / Registers	✓

2. CMT211xA Schematics Guidelines

The CMT211xA devices are parts of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. Considering the balancing between harmonics rejection performance and cost, CMOSTEK recommends using a 3rd-order to 7th-order low-pass filter to build the matching network. Several examples of 315/433.92/868.35/915 MHz, FCC/ETSI compliant or low cost application are given below.

2.1 General Schematic of CMT211xA Application

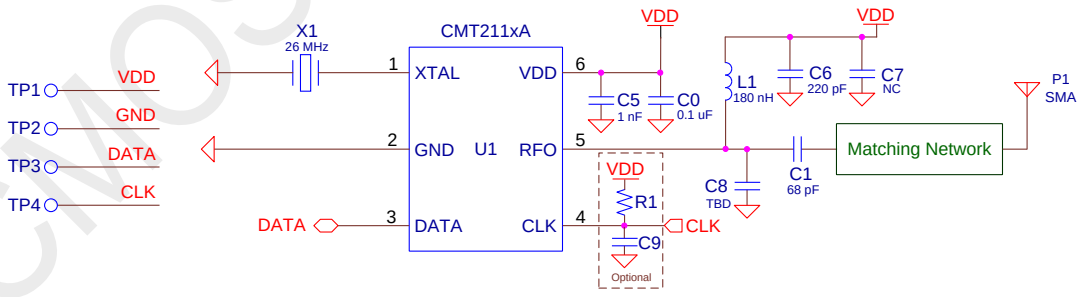

Figure 1. CMT211xA General Application Schematic

Notes:

1. A general schematic of CMT211xA application is shown in the figure above. According to the different application requirements, the low-pass filter for matching network can be different. Details will be given in the following sections.
2. C0, C5, C6 and C7 are the power supply decoupling capacitors. C7 is an optional decoupling capacitor for the PA power supply depending on the power supply purity level.
3. L1 is a choke inductor.

4. The user is recommended to use the two-wire interface (TWI) to control the transmission for power saving and reliability purpose, refer to the datasheet for details of the TWI interface.
   - If 1-wire interface is used to control the transmission while EEPROM programming is required during manufacturing phase, a 1.5 kΩ pull-up resistor R1 and 1 nF capacitor C9 are recommended to tie on CLK pin which helps to enhance the transmission robustness. Both the resistor and capacitor values are good enough for CMOSTEK USB Programmer to drive the CLK pin. When other Programmer is used, R1 and C9 should be properly selected to ensure the EEPROM can be reliably programmed.
   - If the chip's default settings meet the application requirement, then EEPROM programming is not required anymore. In this case, directly tying the CLK pin to VDD is recommended.
5. There are 2 methods to adjust the output power:
   - Configuring the output power of the chip via RFPDK and USB Programmer.
   - Putting a serial connected resistor between the power supply and the choke inductor. The output power is changed by adjusting the value of the resistor.
6. C8 is an optional capacitor. If the matching network built by the standard components meets the application requirement, the user can ignore the C8; otherwise, the C8 can be added to adjust the matching network for better performance.
7. C1 is an AC coupling capacitor.
8. For EEPROM programming, test points (TP1/2/3/4 connected to VDD, GND, DATA and CLK respectively) must be reserved.
9. The integrated crystal oscillator is a single-ended design. The required load capacitance is integrated on-chip to minimize the number of external components. Only a 26 MHz crystal is required. The recommended characteristics of the crystal are:
   - ESR < 60 Ω.
   - Load capacitance from 12 pF to 20 pF.
   - Total tolerance (including the factors of initial tolerance, crystal loading, aging, and temperature change) should be within ±20 ppm typically. The acceptable tolerance depends on RF frequency and channel spacing/bandwidth.
10. An external clock source can easily be used in place of a conventional XTAL. The incoming clock signal is recommended to have a peak-to-peak swing in the range of 300 mV to 700 mV and AC-coupled to the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value on the RFPDK.
11. P1 is a SMA connector for a 50 Ω antenna.

2.2 CMT211xA 315 MHz 3C Compliant Application

2.2.1 Schematic of 315 MHz 3C Compliant Application

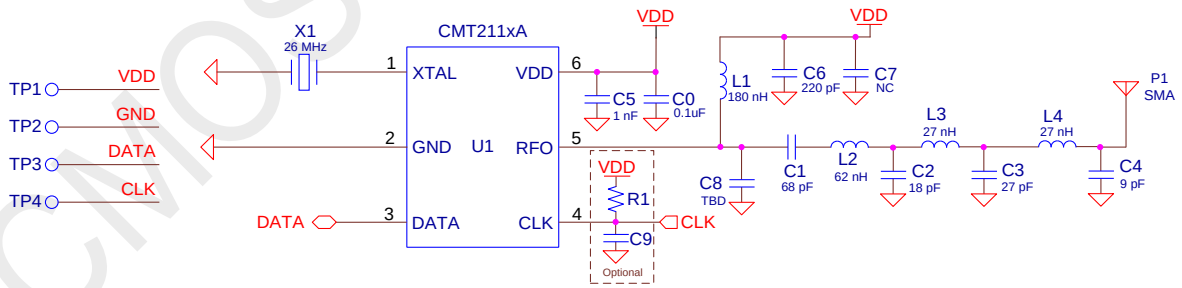

Figure 2. CMT211xA 315 MHz 3C Compliant Application Schematic

Notes:

1. Some of the markets have very strict limitation (e.g. 3C in China) on the 2nd harmonics emission. CMOSTEK recommends using a 7th-order low-pass filter to build the matching network in order to meet these requirements.
2. The output of the PA can be modeled as a shunt resistor R_{INT} in parallel with a shunt capacitor C_{INT} (R_{INT} = 150 Ω and C_{INT} = 6.3 pF @ 315 MHz).
3. L2, L3, L4, C2, C3, C4 and the internal shunt capacitor C_{INT} form a 7th-order low-pass filter as matching network, which transforms the antenna impedance to the load impedance seen at the RFO pin of the CMT211xA.

2.2.2 BOM of 315 MHz 3C Compliant Application

Table 2. BOM of 315 MHz 3C Compliant Applications

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT211xA, low-cost 240 – 960 MHz (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
R1	Optional pull-up resistor on CLK pin	1.5	kΩ	Samsung
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	18	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	27	pF	Murata GRM15
C4	±5%, 0402 NP0, 50 V	9	pF	Murata GRM15
C5	±5%, 0402 NP0, 50 V	1	nF	Murata GRM15
C6	±5%, 0402 NP0, 50 V	220	pF	Murata GRM15
C7	±5%, 0402 NP0, 50 V, optional	0.1	uF	Murata GRM15
C9	Optional capacitor on the CLK pin	1	nF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	62	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	27	nH	Murata LQG18
L4	±5%, 0603 multi-layer chip inductor	27	nH	Murata LQG18

2.3 CMT211xA 315 MHz FCC Compliant Application

2.3.1 Schematic of 315 MHz FCC Compliant Application

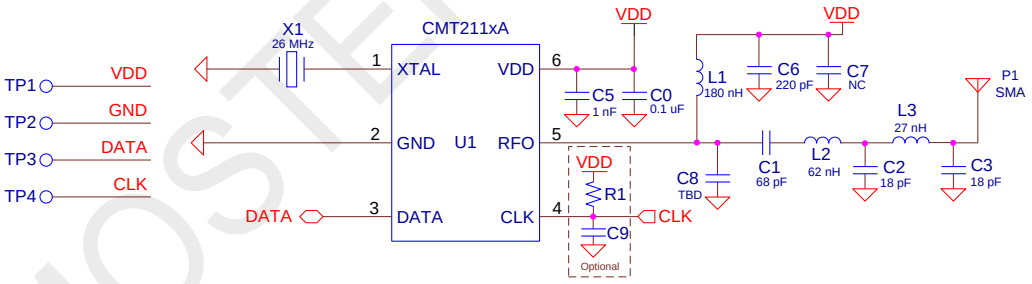

Figure 3. CMT211xA 315 MHz FCC Compliant Application Schematic

Notes:

1. The markets with FCC standard are having lower requirements on the harmonics emission than that of 3C standard. Therefore, CMOSTEK recommends using a 5th-order low-pass filter to build the matching network in order to meet the FCC requirement.
2. The output of the PA can be modeled as a shunt resistor R_{INT} in parallel with a shunt capacitor C_{INT} (R_{INT} = 150 Ω and C_{INT} = 6.3 pF @ 315 MHz).
3. L2, L3, C2, C3 and the internal shunt capacitor C_{INT} form a 5th-order low-pass filter as matching network, which transforms the antenna impedance to the load impedance seen at the RFO pin of the CMT211xA.

2.3.2 BOM of 315 MHz FCC Compliant Application

Table 3. BOM of 315 MHz FCC Compliant Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT211xA, low-cost 240 – 960 MHz (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
R1	Optional pull-up resistor on CLK pin	1.5	kΩ	Samsung
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	18	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	18	pF	Murata GRM15
C5	±5%, 0402 NP0, 50 V	1	nF	Murata GRM15
C6	±5%, 0402 NP0, 50 V	220	pF	Murata GRM15
C7	±5%, 0402 NP0, 50 V, optional	0.1	uF	Murata GRM15
C9	Optional capacitor on the CLK pin	1	nF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	62	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	27	nH	Murata LQG18

2.4 CMT211xA 433.92/868.35/915 MHz FCC/ETSI Compliant Application

2.4.1 Schematic of 433.92/868.35/915 MHz FCC/ETSI Compliant Application

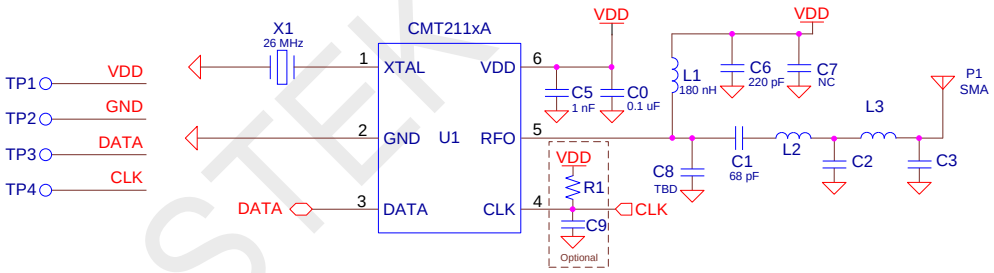

Figure 4. CMT211xA 433.92/868.35/915 MHz FCC/ETSI Compliant Application Schematic

Notes:

1. The frequency of 433.92/868.35/915 MHz is widely used in the global market. In order to meet the FCC/ETSI requirements, a 5th-order low-pass filter is recommended for building the matching network.
2. The output of the PA can be modeled as a shunt resistor R_{INT} in parallel with a shunt capacitor C_{INT}, at the below frequencies, the equivalent value of the R_{INT} and C_{INT} are shown as below.

Table 4. The Equivalent R_{INT} and C_{INT} at PA Output

Frequency (MHz)	R_{INT} (Ω)	C_{INT} (pF)
433.92	120	6.8
868.35	90	7.2
915	80	7.4

3. L2, L3, C2, C3 and the internal shunt capacitor C_{INT} form a 5th-order low-pass filter as matching network, which transforms the antenna impedance to the load impedance seen at the RFO pin of the CMT211xA.

2.4.2 BOM of 433.92/868.35/915 MHz FCC/ETSI Compliant Application

Table 5. BOM of 433.92/868.35/915 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value			Unit	Manufacturer
		433.92 MHz	868.35 MHz	915 MHz		
U1	CMT211xA, low-cost 240 – 960 MHz (G)FSK/OOK transmitter	-			-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26			MHz	EPSON
R1	Optional pull-up resistor on CLK pin	1.5			kΩ	Samsung
C0	±20%, 0402 X7R, 25 V	0.1			uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	68	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	15	9.1	10	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	15	8.2	5.1	pF	Murata GRM15
C5	±5%, 0402 NP0, 50 V	1	1	1	nF	Murata GRM15
C6	±5%, 0402 NP0, 50 V	220	220	220	pF	Murata GRM15
C7	±5%, 0402 NP0, 50 V, optional	0.1	0.1	0.1	uF	Murata GRM15
C9	Optional capacitor on the CLK pin	1	1	1	nF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	100	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	36	8.2	5.6	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	18	8.2	8.2	nH	Murata LQG18

2.5 CMT211xA MHz Low-Cost Applications

2.5.1 Schematic of Low-Cost Applications

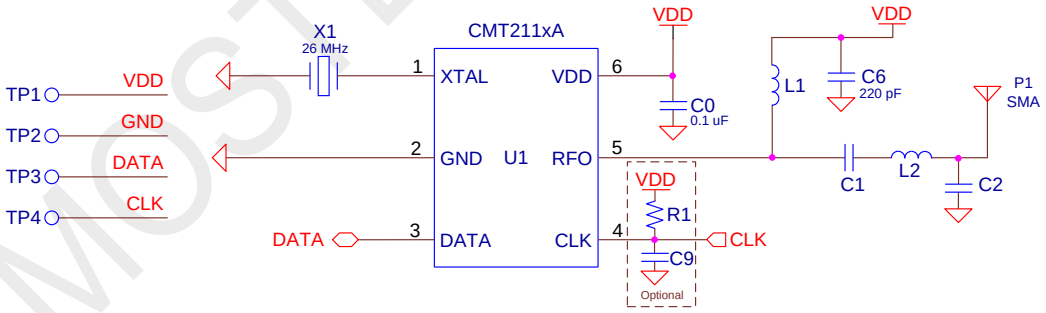

Figure 5. CMT211xA Low-Cost Application Schematic

Notes:

1. For the cost-sensitive applications, the user can use the schematic shown in figure above.
2. The output of the PA can be modeled as a shunt resistor R_{INT} in parallel with a shunt capacitor C_{INT}, and their values are listed in table below.

Table 6. Values of Equivalent RC Parallel Circuit at 315/433.92/868.35/915 MHz

No.	Frequency (MHz)	R_{INT} (Ω)	C_{INT} (pF)
1	315	150	6.3
2	433.92	120	6.8
3	868.35	90	7.2
4	915	80	7.4

3. C0 and C6 are decoupling capacitors for the power supply. Comparing to the scheme in Figure 1, C5 and C7 are eliminated for cost-saving purpose.
4. L2, C2 and the internal shunt capacitor C_{INT} form a 3rd-order low-pass filter as matching network, which transforms the antenna impedance to the load impedance seen at the RFO pin of the CMT211xA.

2.5.2 BOM of Low-Cost Applications

Table 7. BOM of Low-Cost Applications

Designator	Descriptions	Value				Unit	Manufacturer
		315 MHz	433.92 MHz	868.35 MHz	915 MHz		
U1	CMT211xA, low-cost 240 – 960 MHz (G)FSK/OOK transmitter	-				-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26				MHz	EPSON
R1	Optional pull-up resistor on CLK pin	1.5				kΩ	Samsung
L1	±5%, 0603 multi-layer chip inductor	180	180	100	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	47	27	8.2	6.8	nH	Murata LQG18
C0	±20%, 0402 X7R, 25 V	0.1	0.1	0.1	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	82	82	82	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	10	9	3.9	3.9	pF	Murata GRM15
C6	±5%, 0402 NP0, 50 V	220	220	220	220	pF	Murata GRM15
C9	Optional capacitor on the CLK pin	1	1	1	1	nF	Murata GRM15

3. CMT211xA PCB Layout Guidelines

The CMT2110A, CMT2113A, CMT2117A and CMT2119A employ the same package, thus the PCB layouts should follow the same rules. The following PCB layout design guidelines take the CMT2110A-EM as an example.

CMT2110A-EM is a 2-layer PCB using FR4 PCB material. The thickness of the PCB is 0.8 mm; the thickness for the copper is 1 ounce (0.0356mm); the separation between ground pour copper and traces/pads is 0.3 mm; the dielectric constant (Er) for the FR4 material is 4.4. In general, the impedance of the coplanar transmission line is in proportion to the thickness of the PCB and the distance between the routing and grounding around it. It is in inverse proportion to the width/thickness of the routing and the dielectric constant (Er). With the help of a conventional transmission line calculator (such as Txline), a 1-mm width of the 50 Ω coplanar transmission line can be obtained.

3.1 CMT2110A-EM PCB Layout

The PCB layout has five major sections. They are RF Output, Decoupling, XTAL, Digital Signals Routing and Grounding.

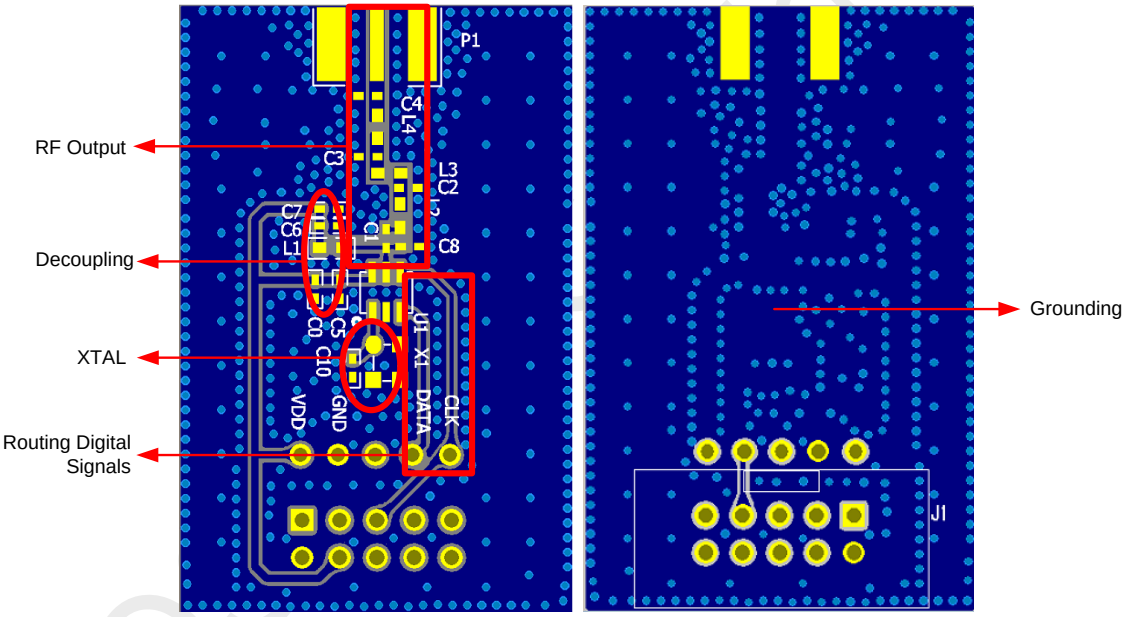

Figure 6. CMT2110A-EM PCB Layout

3.1.1 RF Output

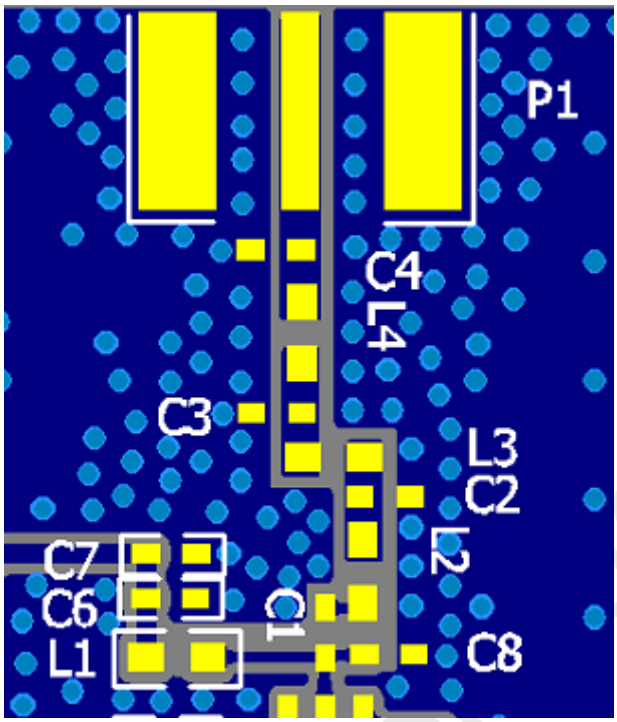

Figure 7. RF Output

The RF output section is shown in figure above.

1. Keep the RF signal routing as straight as possible to minimize the loss of output power. Avoid placing the adjacent inductors in the same orientation to reduce the coupling between them.
2. Place L1 as close to the RFO pin as possible.
3. The matching network should be placed as close to the CMT2110A as possible.
4. Since the impedance at the RFO pin is about 150 Ω, a 0.2-mm width transmission line between the L2 and CMT2110A is used. The width of the transmission line is 1 mm between L2 and the SMA connector which is of 50 Ω impedance.
5. Do not place any silk print on any RF components, as the silk print can impact the dielectric constant (Er) of the PCB, as well as the PA output impedance.
6. The ground pour flooding and the RF signal routing should be smooth to avoid the impedance variation on the transmission lines, which will result in RF signal reflection and performance inconsistency in mass production.
7. P1 is a SMA connector for the antenna. The monopole antenna is a very popular antenna which most commonly refers to a quarter-wavelength (λ/4). One antenna element is one λ/4 wavelength and the GND plane acts as the other λ/4 wavelength which produces an effective λ/2 antenna. Therefore, for monopole antenna designs the performance of the antenna depends on the ground size. Considering cost, performance and time-to-market, the user can choose different types of monopole antenna, including PCB antenna, chip antenna, whip antenna or wire antenna. CMT2110A-EM uses a whip antenna for optimal RF performance.

3.1.2 Decoupling

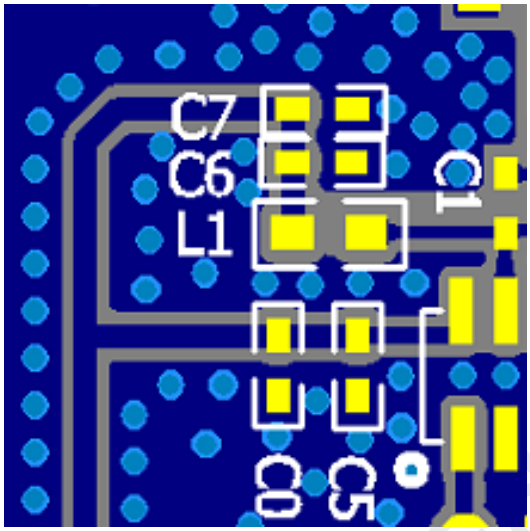

Figure 8. Decoupling

1. Place C6 and C7 as close to L1 as possible to isolate the power supply from the PA output.
2. Place C0 and C5 as close to the power supply of CMT2110A as possible.

3.1.3 XTAL

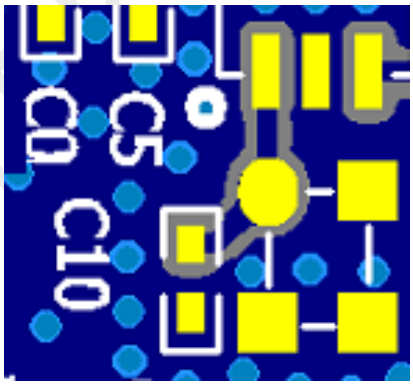

Figure 9. XTAL

The XTAL should be placed as close to the CMT2110A as possible to ensure that wire parasitic capacitances are minimized. This reduces any frequency offsets that may occur. C10 is a capacitor for CMOSTEK internal use only. The user does not need to include it in the design.

3.1.4 Digital Signals Routing

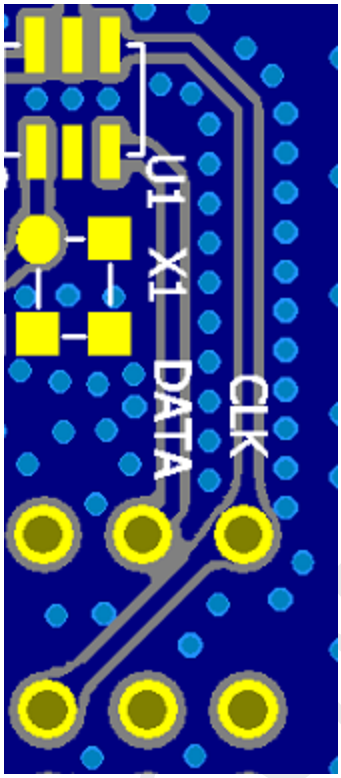

Figure 10. Digital Signals Routing

The digital signals must be routed away from both of the RF and the XTAL signals to avoid high frequency harmonics coupling to those sensitive signals. The solid ground should be placed between the DATA and CLK signal routings to avoid cross-coupling.

3.1.5 Grounding

1. Use as much continuous ground plane metallization as possible.
2. Place a series of ground vias along the PCB edges if possible. The maximum distance between the vias should be less than λ/10. This is required to reduce the PCB radiation at higher harmonics caused by the fringing field of routing edges.

4. Document Change List

Table 8. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.9	All	Initial released version	2014-06-14
1.0	-	-	2014-06-30
1.1	All	Add CMT2113/17/19A to the document	2015-02-11

5. Contact Information

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